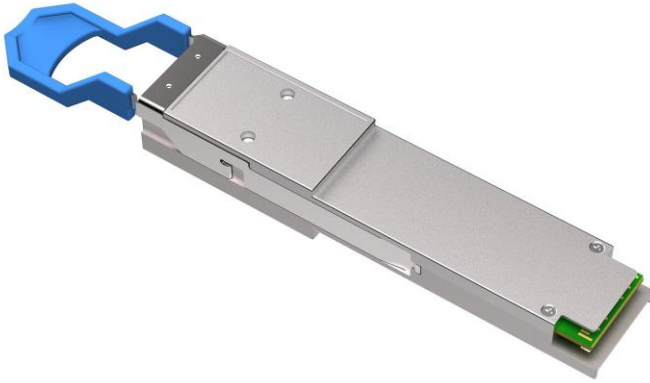


400G QSFP112 DR4 LPO Optical Transceiver (STC-40004) Datasheet



Applications:

- ▶ 400G Ethernet
- ▶ Data Center Interconnect
- ▶ Infiniband Interconnect
- ▶ Enterprise Networking

Standards

- ▶ Compliant with LPO MSA 100G-DR-LPO Draft Revision 0.5 optical specifications
- ▶ Compliant with CEI-112G-LINEAR-PAM4 electrical specifications
- ▶ Form factor of QSFP112 type2(87.4mm)
- ▶ MPO12 receptacle with APC end face
- ▶ 4x106.25Gb/s electrical interface (400GAUI-4)
- ▶ Up to 0.5km transmission on single mode fiber (SMF) with FEC
- ▶ Single +3.3V power supply
- ▶ Case temperature range: 0 ~ +70°C
- ▶ Maximum power consumption 6W
- ▶ RoHS 2.0 complaint

Description:

SWEDISH TELECOM OPTO's STC-40004 a 400Gb/s QSFP112 optical module designed for 0.5Km optical communication applications. The module converts 4 channels of 100Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s.

On the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each

channel for an aggregate data rate of 400Gb/s into 4 channels of 100Gb/s (PAM4) electrical output data. An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP112 DR4 module receptacle. Host FEC is required to support up to 0.5Km fiber transmission.

► Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	TSTG	-40	+85	°C
Supply Voltage	VCC	-0.5	3.6	V
Relative Humidity	RH	10% to 90% non-condensing		

► Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Case Temperature- Operating	T _{CASE}	0	70	°C
Supply Voltage	V _{CC}	3.135	3.465	V
Power Consumption	P _{DISS}		6	W
Pre-FEC Bit Error Ratio			2.4x10 ⁻⁴	
Post-FEC Bit Error Ratio			1x10 ⁻¹²	
Link Distance			500	M

► Transmitter Optical Specifications

Transmitter Parameter	Min	Typical	Max	Unit
Signaling rate each lane		53.125		GBd
Lane Wavelength Range	1304.5	1310	1317.5	nm
Modulation Format	PAM4			
Average Optical Power per lane	-2.9		4	dBm
Outer Optical Modulation Amplitude (OMA _{outer}), each lane	-0.8		4.2	dBm
Average Launch Power per Lane @ TX Off State			-15	dBm
Launch Power in OMA _{outer} minus TDECQ, each Lane	-2.2			dB
Transmitter and Dispersion Eye Closure for PAM4, each Lane			3.4	dB
Extinction Ratio	3.5			dB
Relative Intensity Noise _{21.4} (OMA)			-136	dB/Hz
Side-Mode Suppression Ration (SMSR)	30			dB
Optical Return Loss Tolerance			21.4	dB
Transmitter Reflectance			-26	dB

► Receiver Optical Specifications

Receiver Parameter	Min	Typical	Max	Unit	Note
Signaling rate each lane		53.125		GBd	
Lane Wavelength Range	1304.5	1310	1317.5	nm	
Modulation Format	PAM4				
Damage Threshold	5			dBm	
Average Receive Power, each lane	-5.9		4	dBm	
Receiver Power, each lane (OMA)			4.2	dBm	
Receiver Reflectance			-26	dB	
Receiver Sensitivity each lane (OMA _{outer})			Equation	dBm	1
Stressed Receiver Sensitivity (OMA _{outer}), each			-1.9	dBm	
Stressed Conditions for Stress Receiver Sensitivity					
Stressed Eye Closure for PAM4 (SECQ), Lane under Test		3.4		dB	
OMA _{outer} of each Aggressor Lane		4.2		dBm	
1. Receiver sensitivity (OMA _{outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. It should meet Equation: $RS = \max(-3.9, -SECQ/5.3)$, where RS is the receiver sensitivity, and SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.					

► Receiver Thresholds for Loss of Signal (LOS)

Parameter	Min	Typical	Max	Unit
RX_LOS_Assert Min/Max	-24.0			dBm
RX_LOS_De-Assert Min/Max			-13	dBm
RX_LOS_Hysteresis		1.5		dB

► Digital Diagnostic Monitoring Specifications

Parameter	Unit	Specification
Temperature Monitor absolute error	°C	±3
Supply Voltage Monitor absolute error	%	±5
I _{bias} Monitor absolute error	%	±10
Received Power (Rx) Monitor absolute error	dB	±3.00
Transmit Power (Tx) Monitor absolute error	dB	±3.00

► Low Speed Electrical signal

Parameter	Symbol	Min	Max	Units	Condition
SCL and SDA	VOL	0	0.4	V	IOL (max)=3.0mA for fast mode, 20mA for Fast-mode plus
	VOH	V _{cc} -0.5	V _{cc} +0.3	V	
SCL and SDA	VIL	-0.3	V _{cc} *0.3	V	

	VIH	Vcc*0.7	Vcc +0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0k Ohms Pull up resistor,max
			200	pF	1.6k Ohms Pull up resistor,max
LPMode/TxDis,Reset and ModeSel	VIL	-0.3	0.8	V	Iin <= 125uA for Vin < Vcc
	VIH	2	Vcc + 0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC - 0.5	VCC + 0.3	V	10k ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	%	IOL=2.0mA
	VOH			dB	ModPrsL can be implemented as a short- circuit to GND on the module

► High Speed Electrical signal

Parameter	Min	Max	Unit	Conditions
Receiver electrical output characteristics at TP4				
Differential Voltage, pk-pk	300 300	700 600	mV mV	Host can request voltage level within these values. Initialization value
VMA	250	500	mV	See Section 29.3.6
Common Mode Voltage (Vcm)	-350	2850	mV	See Note 1
Peak to Peak AC Common Mode Voltage Low Frequency (VCMLF)	-	30	mV	See Note 1
Peak to Peak AC Common Mode Voltage Full Band (VCMFB)	-	80	mV	See Section 29.3.7
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz. See Section 13.3.6
Common Mode to Differential Mode Conversion (SDC22)	-	Equation 29-2	dB	See Note 2
Effective Return Loss (ERL)	9	-	dB	See Section 29.3.9
Common Mode Return Loss (SCC22)	-	-2	dB	From 250 MHz to min(0.8*fb, 43 GHz) See Note 2
EECQ (SMF)		8	dB	See Section 29.4.1.2 See Note 3

EECQ (MMF)		10	dB	See Section 29.4.1.2 See Note 3
NOTES: Vcm is generated by the host. Specification includes effects of ground offset voltage. S-parameter specifications are based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω Open eye is generated through the use of a reference Continuous Time Linear Equalizer (CTLE), 22 tap FFE and 1 tap DFE applicable to all three PAM4 eyes (See 29.4.1.2)				
Parameter	Min	Max	Unit	Conditions
Transmitter electrical input characteristics at TP1				
Overload Differential Voltage	525	-	mV	See 29.4.2
Common Mode Voltage (Vcm)	-0.3	2.8	V	See Notes 1, 2
Differential Termination Resistance Mismatch	-	10	%	At 1 MHz. See 29.3.8
Differential Mode to Common Mode Conversion (SCD11)	-	Equation 29-1	dB	See Note 2
Effective Return Loss (ERL)	9	-	dB	See Section 29.3.9
Stressed Input Test	See Section 29.4.1.3			
NOTES: Vcm is defined in Table 1-2 General Definitions of Section 1.6 Vcm is generated by the host. Specification includes effects of ground offset voltage S-parameter specifications are based on a differential reference impedance of 100Ω and a common mode reference impedance of 25Ω				

► Module Block Diagram

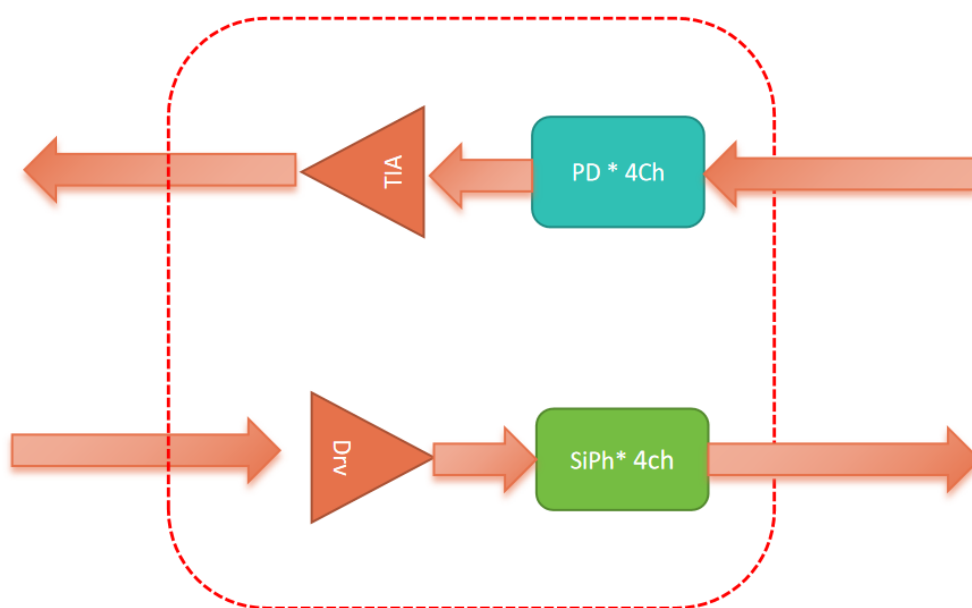


Figure 1. Module Block Diagram

► OSFP800 Edge Connector and Pinout Description

The electrical pinout of the QSFP112 module is shown in Figure 2 below.

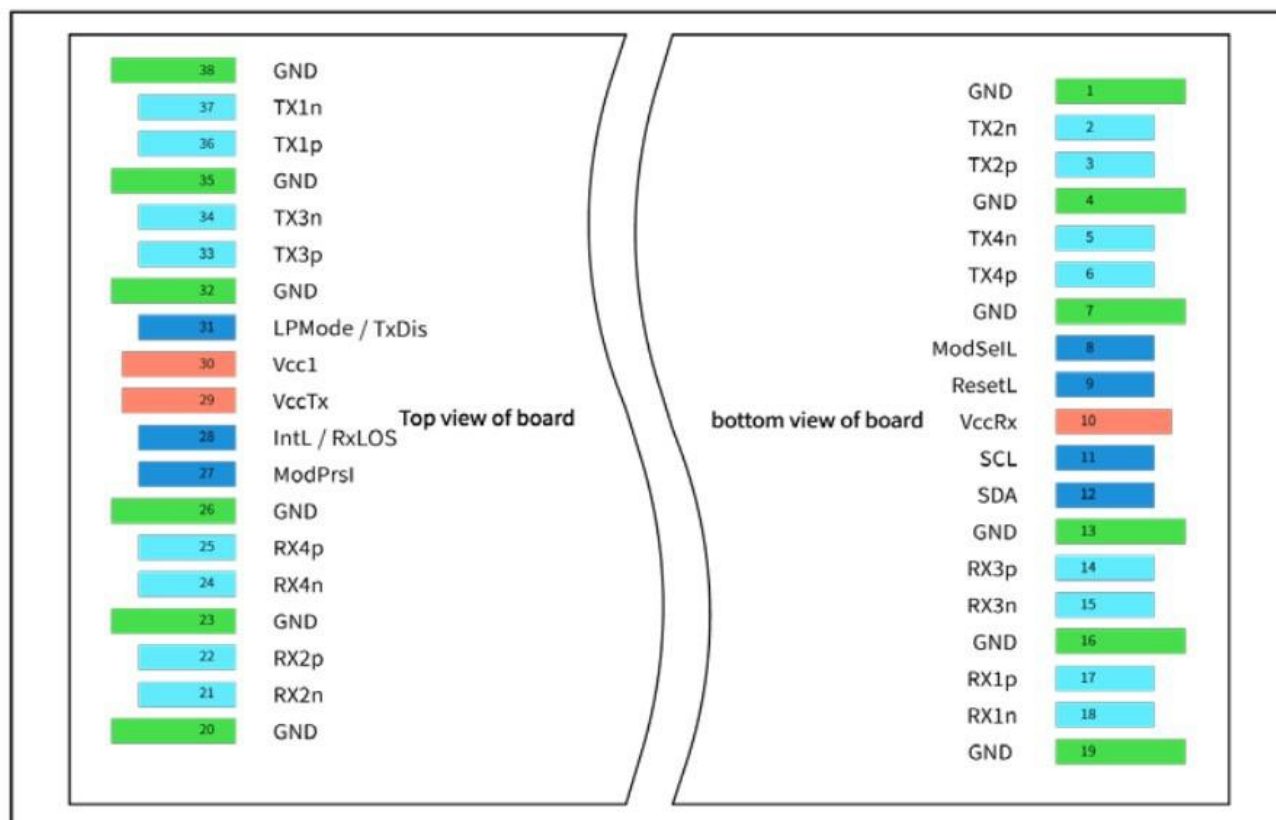


Figure 2. QSFP112 module contact assignment

► Module contact definition

Pin No.	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	TX2n	Transmitted Inverted Data Input	3	
3	CML-I	TX2p	Transmitted Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	TX4n	Transmitted Inverted Data Input	3	
6	CML-I	TX4p	Transmitted Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSeil	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3 VDC Receiver Power Supply	2	2
11	LVC MOS -I/O	SCL	Serial Clock for I2C Interface	3	
12	LVC MOS -I/O	SDA	Serial Data for I2C Interface	3	
13		GND	Ground	1	1

Pin No.	Logic	Symbol	Description	Plug Sequence	Notes
14	CML-O	RX3p	Receiver Non-Inverted Data Output	3	
15	CML-O	RX3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	RX1p	Receiver Non-Inverted Data Output	3	
18	CML-O	RX1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	RX2n	Receiver Inverted Data Output	3	
22	CML-O	RX2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	RX4n	Receiver Inverted Data Output	3	
25	CML-O	RX4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxL OS	Interrupt/optional RxLOS	3	
29		Vcc Tx	+3.3 VDC Transmitter Power Supply	2	2
30		Vcc1	+3.3 VDC Power Supply	2	2
31	LVTTL-I	LPMode/Tx dis	Low Power Mode/optioanl Tx Disable	3	
32		GND	Ground	1	1
33	CML-I	TX3p	Transmitted Non-Inverted Data Input	3	
34	CML-I	TX3n	Transmitted Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	TX1p	Transmitted Non-Inverted Data Input	3	
37	CML-I	TX1n	Transmitted Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements, defined for the host side of the Host Edge Card Connector, are listed in Table 4. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for

Pin No.	Logic	Symbol	Description	Plug Sequence	Notes
high module power of 15-20W).					

► Optical interface

The four transmit and four receive optical lanes of the module occupy the positions depicted in Figure 3 when looking into the MPO12 receptacle with the connector keyway feature on top. The interface contains eight active lanes within twelve total positions. The transmit optical lanes occupy the left-most four positions. The receive optical lanes occupy the right-most four positions. The four center positions are unused. To minimize MPO connection induced reflections, a MPO receptacle with 8-degree angled end-face is utilized for this product.

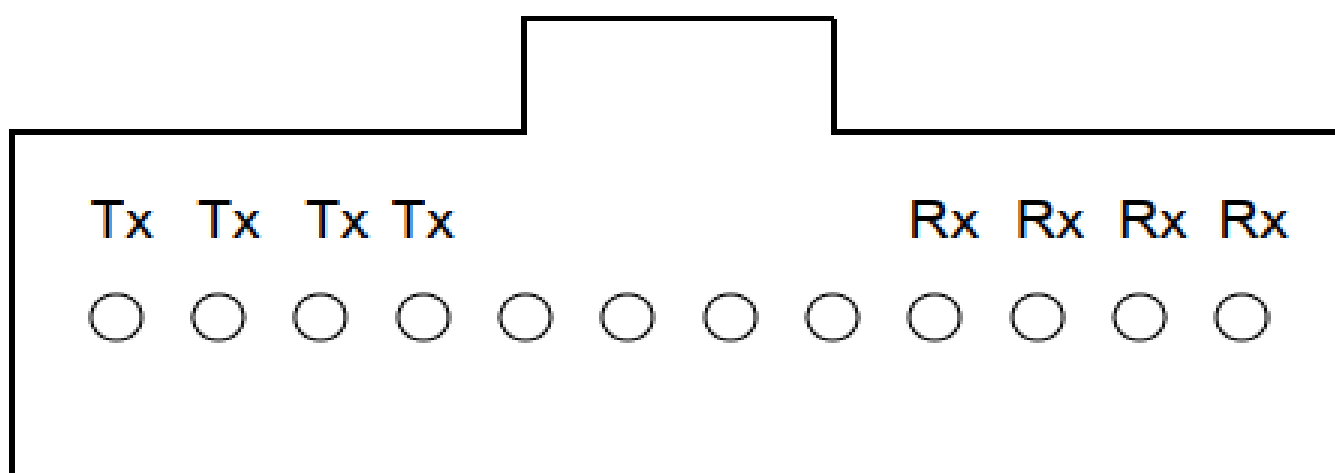


Figure 3. Optical lane assignments

► Mechanical Specifications

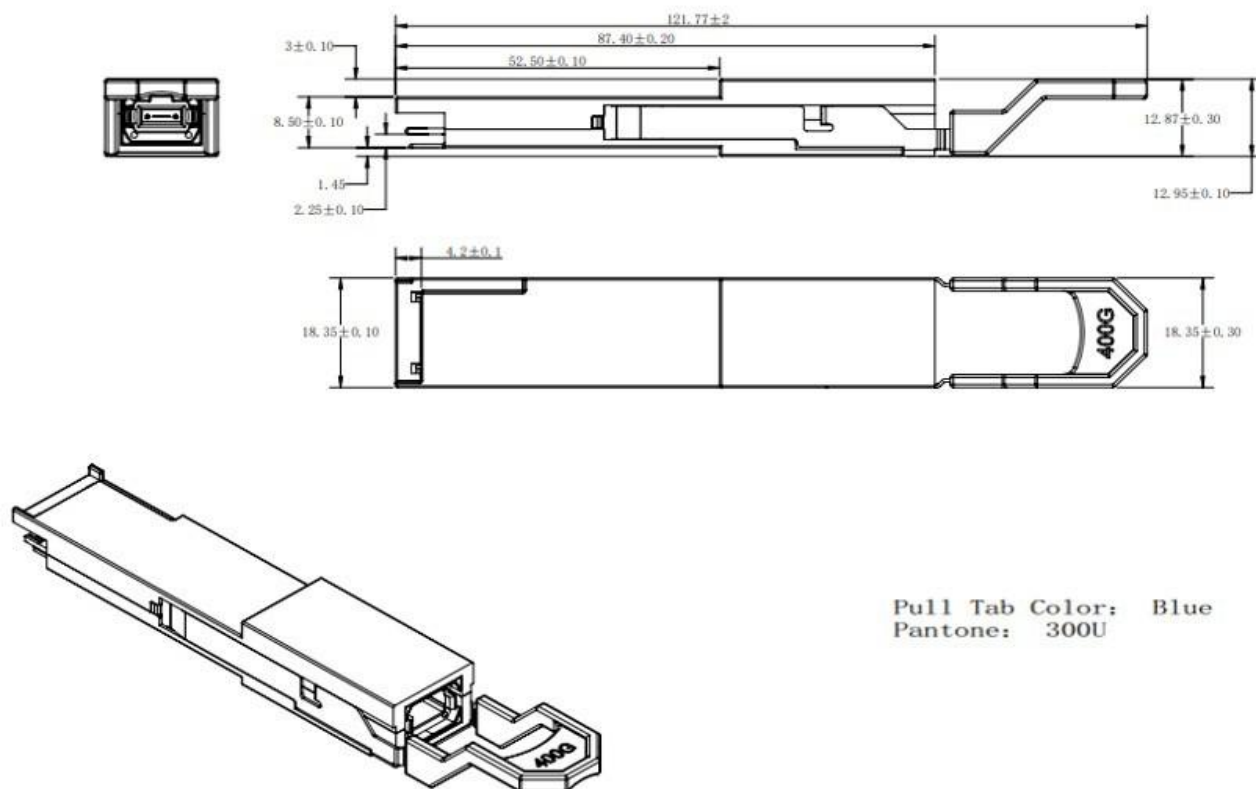


Figure 4. Mechanical Dimensions

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