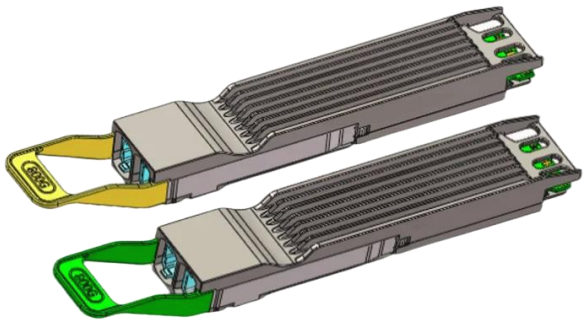
800G Linear OSFP112 DR8 (LPO) Transceiver (STC-40016) Datasheet



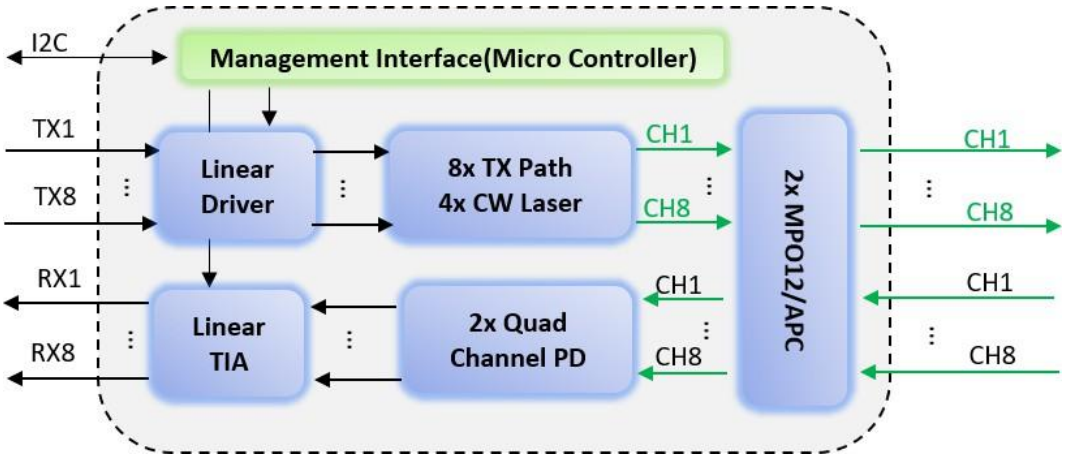
1. Introduction

This product is an 800Gb/s Linear Octal Small Form-factor Pluggable (OSFP) optical module with top closed fin designed for low power and low latency 500m optical communication applications. The module converts 8 channels of 100Gb/s (PAM4) electrical input data to 8 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 800Gb/s. Reversely, on the receiver side, the module converts 8 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 800Gb/s into 8 channels of 100Gb/s (PAM4) electrical output data. Linear driver and TIA is used to pass through the signal with high quality without retimer.

An optical fiber cable with dual MPO-12 connector can be plugged into the OSFP112 DR8 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an OSFP MSA-compliant edge type connector.

I2C interface is supported to read and control the status of this product.

Figure 1 shows the transceiver block diagram



- OSFP form factor hot pluggable
- CMIS compliance
- 8 independence parallel optical channels
- Up to 53.125GBaud per lane
- Dual optical port of MPO-12/APC
- 500m maximum reach via single mode fiber
- 9 Watts max
- Case temperature range of 0°C to 70°C

2. Key Features

The transceiver complies with common management interface specification (CMIS). The supported key features listed below allow host software to read and control the transceiver status through I2C.

- Supply voltage monitoring (DDM_Voltage)
- Transceiver case temperature monitoring (DDM_Temperature)
- Tx transmit optical power monitoring for each lane (DDM_TxPower)
- Tx bias current monitoring for each lane (DDM_TxBias)
- Rx receive optical power monitoring for each lane (DDM_RxPower)
- Loss of modulation monitoring for each lane (LOM)
- Warning and alarm indication for each DDM function
- Tx fault indication
- CDB firmware upgrade capability

3. Pin Map and Description

The electrical interface of OSFP module consist of a 60 contacts edge connector as illustrated by the diagram in Figure 2, which defined in Clause 8.1 of OSFP MSA Specification.

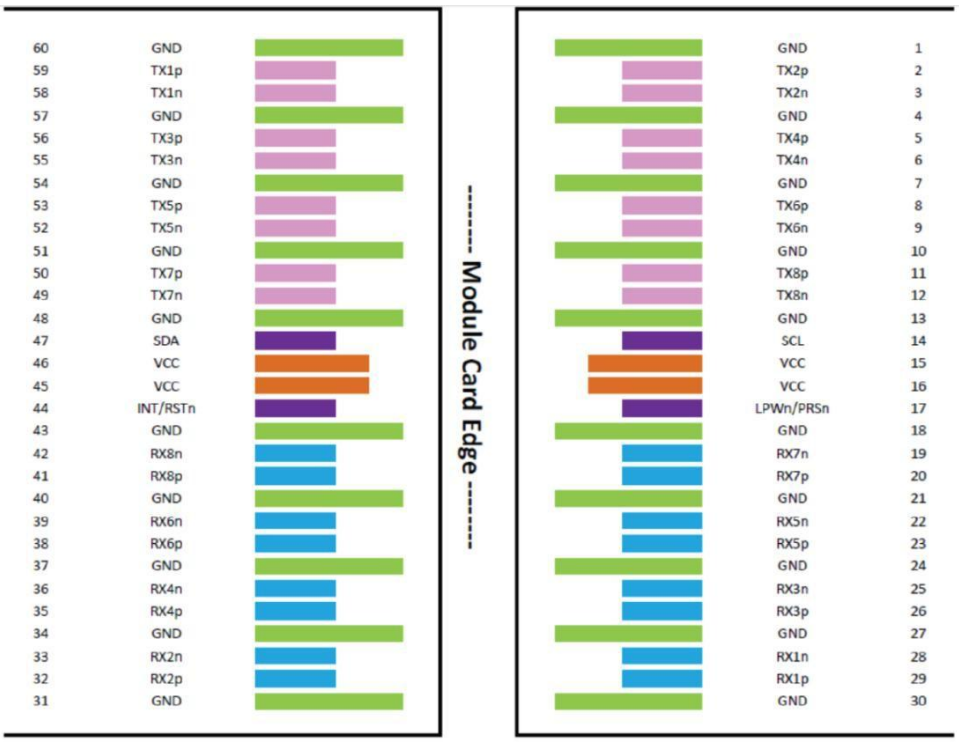


Figure 2. MSA Compliant Connector

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

Table 2 shows the detailed control pins

Table 2. OSFP Control pins

Name	Direction	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	Input/Output	Dual Function Signal . Low Power mode is an active-low input signal . Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal Voltage zones is shown as figure3.
INT/RSTn	Input/Output	Dual Funtion Signal . Reset is an active-low input signal . Interrupt is an active-high output signal Voltage zones is shown as figure 3.

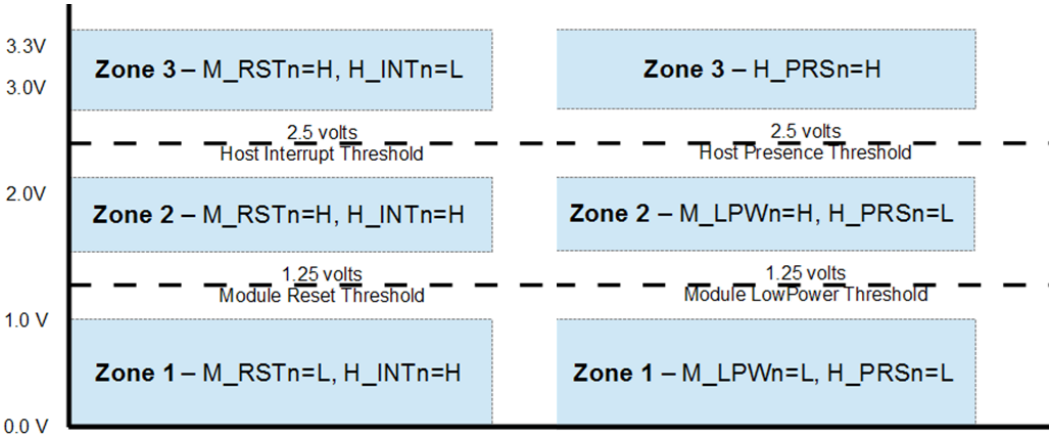


Figure 3. Voltage Zones

Figure 4 shows the recommended power supply filter design

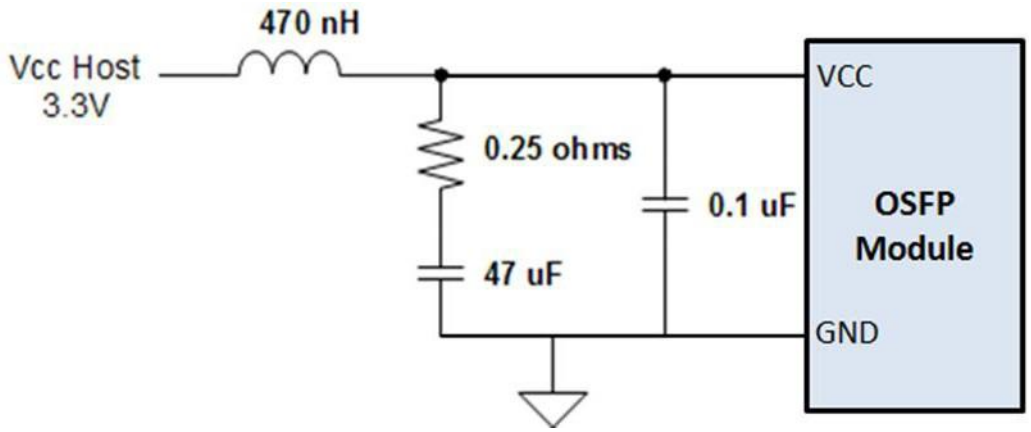


Figure 4. Recommended Power Supply Filter

► 4. Optical Port Description

The optical interface port is dual MPO-12 APC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 5 when looking into the MDI receptacle with the connector keyway feature on top.

Aligned keys are used to ensure alignment between the modules and the patch cords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top. Note: Two alignment pins are present in each receptacle.

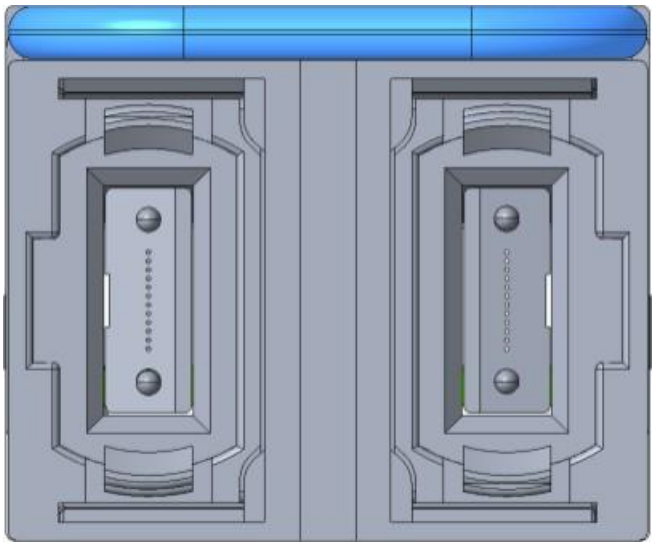


Figure 5. Optical Media Dependent Interface port assignments

► 5. Specification

5.1 Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	TS	-40	85	degC	
Operating Case Temperature	TOP	0	70	degC	
Power Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

5.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	TOP	0		70	degC	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Data Rate, each Lane				53.125	GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-15}$		1
Link Distance	D	2		500	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

5.3 Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				9	W	
Module Input (each Lane)						
Overload Differential Voltage pk-pk	TP1a	525			mV	
Common Mode Voltage	TP1	-0.3		2.8	V	
Differential Termination Resistance Mismatch	TP1			10	%	
Differential Mode to Common Mode Conversion (SCD11)	TP1	Equation 29-1 in CEI-112G- LINEAR -PAM4			dB	
Effective Return Loss (ERL)	TP1	9				
Stress Input Test	TP1a	Section 29.4.1.3				
Module Output (each Lane)						
Differential Peak-to-Peak Output Voltage	TP4	400		600	mV	
Common Mode Voltage	TP4	-350		2850	mV	
Pk-Pk AC Common Mode Voltage Low Frequency	TP4			30	mV	
Pk-Pk AC Common Mode Voltage Full Band	TP4			80	mV	
Differential Termination Resistance Mismatch	TP4			10	%	
Common-mode to Differential mode Conversion	TP4	Equation 29-2 CEI-112G-LINEAR-PAM4			dB	
Effective Return Loss	TP4	9.0			dB	
Common Mode Return Loss	TP4			-2	dB	
EECQ	TP4			8.0	dB	

5.4 Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Center Wavelength	λc	1304.5	1310	1317.5	nm	
Transmitter						
Data Rate, each Lane			53.125 ± 50 ppm		GBd	
Modulation Format			PAM4			
Side-mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	PAVG	-3.9		4	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each Lane	POMA	-1.8		3.2	dBm	
OMA-TDECQ, each Lane		-3.7			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.9	dB	2
Ceq		-0.5		2.5	dB	3
Overshoot/undershoot				25	%	
Outer eye height to inner eye height ratio	EHRu/L	TBD		TBD	%	4
Outer eye height symmetry,	EHS	TBD		TBD	%	5
Extinction Ratio	ER	2.5			dB	
RIN21.5OMA	RIN			-138	dB/Hz	
Optical Return Loss Tolerance	TOL			21.4	dB	
Average Launch Power of OFF Transmitter, each Lane	Poff			-15	dBm	
Receiver						
Data Rate, each Lane			53.125 ± 50 ppm		GBd	
Modulation Format			PAM4			
BER without EC			2.4E-4			
Damage Threshold, each Lane	THd	5			dBm	3

Average Receive Power, each Lane		-6.9		4	dBm	4
Receive Power (OMAouter), each Lane				3.2	dBm	
Receiver Sensitivity (OMAouter), each Lane	SEN			Max (-5.1, -6.5+TDECQ	dBm	5
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS			-2.6	dBm	6
Receiver Reflectance	RR			-26	dB	
LOS Assert	LOSA	-15		-9.9	dBm	
LOS De-assert	LOSD			-6.9	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Conditions of Stress Receiver Sensitivity Test (Note 7)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test				3.9	dB	
OMAouter of each aggressor lane		3.2 A ma			dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. The values for OMA_{outer}(min) vary with TDECQ. Figure 6 illustrates this along with the values for OMA_{outer}(max).
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity (OMA_{outer}) is informative and is defined for a transmitter with a value of TECQ up to
6. 3.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 6.

$$RS = \max(-3.9, TECQ - 5.3)\ dBm \qquad (1)$$

Where:

RS is the receiver sensitivity, and

TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.

7. Measured with conformance test signal at TP3 for the BER equal to 2.4x10-4.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver. A max. SEQC of 3.9 dB is assumed.

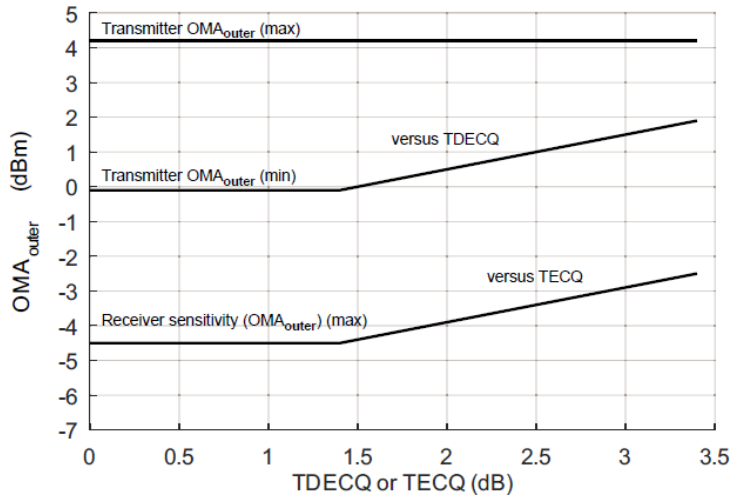


Figure 6. Illustration of Transmitter OMAouter and Receiver Sensitivity Mask for 800G-DR8+

5.5 Digital Diagnostic Specifications

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

► 6. Mechanical Drawing

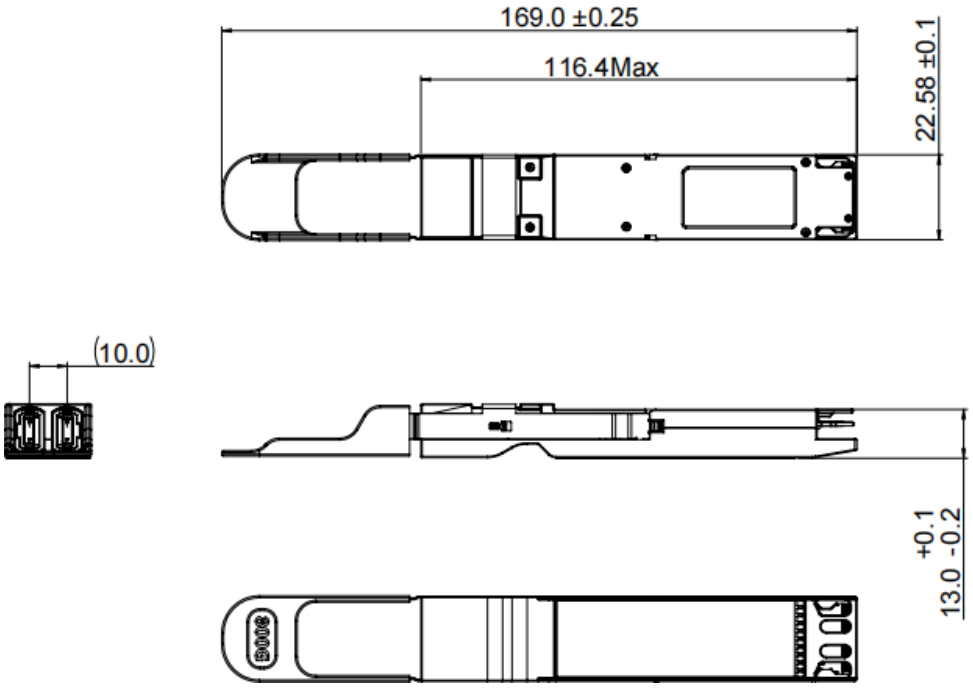


Figure 7. Mechanical Outline

► 7. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

► 8. Laser safety

This is a Class I Laser Product, or Class 1 Laser Product according to IEC/EN 60825-1:2014.

This product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

► Document Revision

Version No.	Date	Reviser	Description
V1.0	2024-01-10	Vincent Ye	Draft