

800G OSFP LPO SR8 Optical Transceiver (STC-40027) Datasheet



- ▶ Hot-pluggable OSFP800 800G form factor
- ▶ Single +3.3V power supply

Applications:

- ▶ Data centers and Cloud Networks

Features:

- ▶ Up to 106 Gbps data rate per channel by PAM4 modulation
- ▶ Support 800GAUI-8 electrical interface
- ▶ Integrated 850nm VCSEL array and PD array
- ▶ w/o DSP or CDR
- ▶ Up to 20m transmission with OM3 MMF
- ▶ Up to 50m transmission with OM4 MMF
- ▶ DDM function implemented

Standards

- ▶ Compliant to OSFP MSA 5.0
- ▶ Compliant with CMIS 4.0
- ▶ Compliant to IEEE P802.3db
- ▶ 8x106. 25Gb/s electrical interface (800GAUI-8)
- ▶ Maximum power consumption 5.5W
- ▶ Single +3.3V power supply
- ▶ Case temperature range: 0 ~ +70°C
- ▶ RoHS 2.0 complaint

Rev	Date	Modified by	Description
A	Nov 15,2022	vic	Initial Release
B	Jul 24,2024	Vic	Update power dissipation and described
C	Aug 29,2024	Vic	Add Electrical、 optical characteristics



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► Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	TSTG	-40	+85	°C
Supply Voltage	VCC	0.5	3.6	V
Relative Humidity	RH	5% to 95% non-condensing		

► Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Case Temperature- Operating	T _{CASE}	0	70	°C
Supply Voltage	V _{CC}	3.135	3.465	V
Power Consumption	P _{DISS}		5.5	W
Pre-FEC Bit Error Ratio			2.4x10 ⁻⁴	
Link Distance over OM3		0.5	20	M
Link Distance over OM4		0.5	50	M

► Optical Specifications

Parameters	Units	Min	Max	Parameters
Tx/Rx signaling rate(each lane)	GBd		53.125	
Tx_AOP	dBm	-4.6	4	PRBS31Q
Tx_OMA (outer)	dBm	-2.6	3.5	PRBS13Q
ER (outer)	dB	2.5		PRBS13Q
TDECQ	dB	Golden sample approved		SSPRQ pattern
OMA-TDECQ	dBm			
Tx/Rx wavelength range	nm	840	870	PRBS31Q
TxDisablePower	dBm		-30	
RIN17.1OMA	dB/Hz		-132	Square Wave
Optical return loss tol.	dB		17.1	
Rx damage threshold	dBm	5		
Stressed_Sen_OMA@2E10-4	dBm	Golden sample approved		PRBS31Q
Rx_AOP	dBm	-6.4	4	PRBS31Q
Rx_OMA	dBm		3.5	PRBS13Q
Sensitivity	dBm	Golden sample approved		-
LOSA (OMA)	dBm	-15	-11	
LOSD (OMA)	dBm	-14	-10	
LOSH (OMA)	dBm	0.5	3	
DMI_VCC	V	3.036	3.565	
DMI_TX_Pwr_Err	dBm	-3	3	
DMI_RX_Pwr_Err	dBm	-3	3	
DMI_Temp_Err	°C	-3	3	
DMI_VCC_Err	V	-0.1	0.1	

► Low Speed Electrical signal

Parameter	Symbol	Min	Max	Units	Condition
SCL and SDA	VOL	0	0.4	V	IOL (max)=3.0mA for fast mode,20mA for Fast-mode plus
	VOH	V _{cc} -0.5	V _{cc} +0.3	V	
SCL and SDA	VIL	-0.3	V _{cc} *0.3	V	
	VIH	V _{cc} *0.7	V _{cc} +0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0k Ohms Pull up resistor,max
			200	pF	1.6k Ohms Pull up resistor,max
V_INT/RSTn_1		0	1	V	for No Module
V_INT/RSTn_2		0	1	V	for Module installed, H_RSTn=Low
V_INT/RSTn_3		1.5	2.25	V	for Module installed, H_RSTn=High,M_INT=Low
V_INT/RSTn_4		2.75	3.465	V	for Module installed, H_RSTn=High,M_INT=High
V_LPWn/PRSn_1		0	1.1	V	for Module installed, H_LPWn=Low
V_LPWn/PRSn_2		1.4	2.25	V	for Module installed, H_LPWn=High
V_LPWn/PRSn_3		2.75	3.465	V	for No Module

► High Speed Electrical signal

Parameter	Min	Typical	Max	Unit	Notes
Receiver electrical output characteristics at TP4					
Signaling rate per lane		53.125		GBd	
AC common-mode output voltage(RMS)		-	17.5	mV	
Differential peak-to-peak output voltage			900	mV	
Near-end Eye height, differential	24			mV	
Near-end vertical eye closure			7.5	dB	
Far-end Eye height, differential	24			mV	
Far-end vertical eye closure			7.5	dB	
Common mode to differential conversion return loss	802.3ck 120G-1				
Effective return loss	8.5			dB	

Differential termination mismatch			10	%	
Transition time (min, 20% to 80%)	8.5			ps	
DC common mode voltage	-350		2850	mV	
Transmitter electrical input characteristics at TP1					
Signaling rate, per lane		53.125		GBd	
Differential pk-pk input voltage tolerance	900			mV	
Common-mode to differential return loss	802.3ck Equation(120G-1)				
Effective return loss	8.5			dB	
Differential termination mismatch			10	%	
Module stressed input test	See 120G.3.4.1				
Single-ended voltage tolerance range	-0.4		3.3	V	
DC common-mode voltage	-350 2850			mV	

► Module Block Diagram

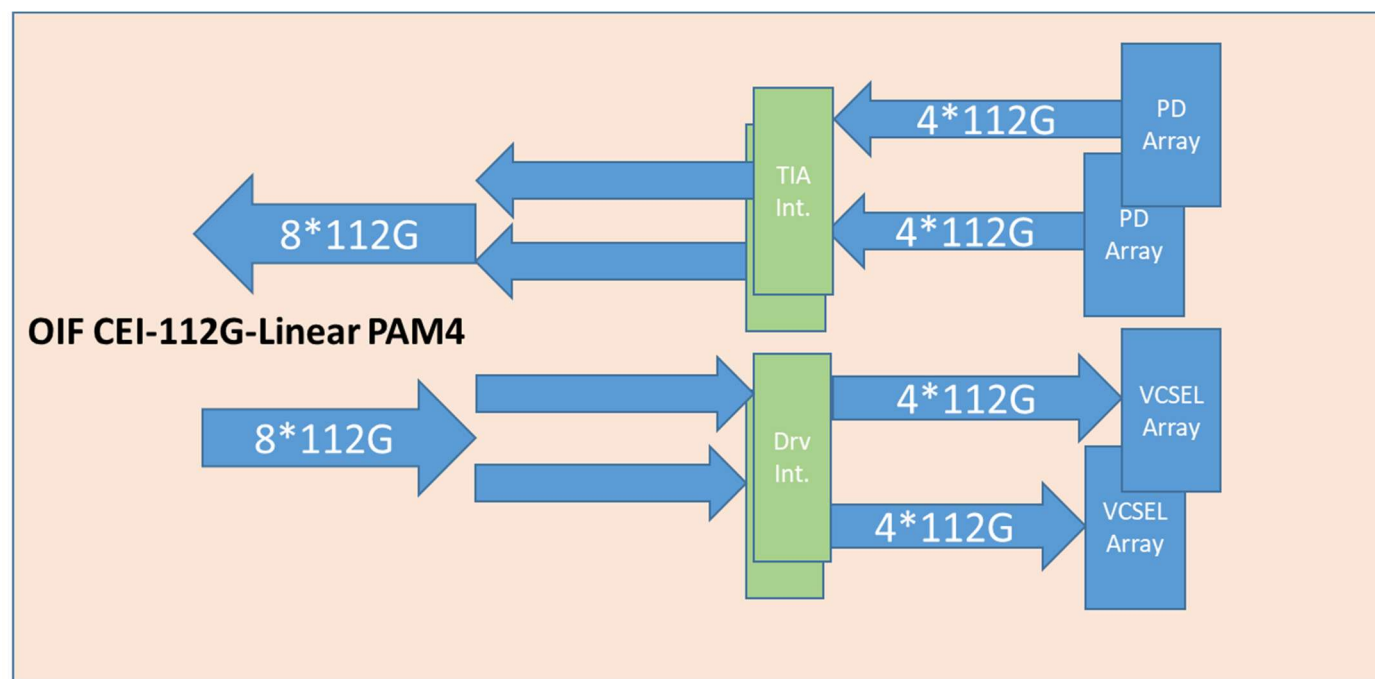


Figure 1 MSA-compliant connector

Module Electrical Connector Pinout

Top Side (viewed from top)

60	GND	
59	TX1p	
58	TX1n	
57	GND	
56	TX3p	
55	TX3n	
54	GND	
53	TX5p	
52	TX5n	
51	GND	
50	TX7p	
49	TX7n	
48	GND	
47	SDA	
46	VCC	
45	VCC	
44	INT/RSTn	
43	GND	
42	RX8n	
41	RX8p	
40	GND	
39	RX6n	
38	RX6p	
37	GND	
36	RX4n	
35	RX4p	
34	GND	
33	RX2n	
32	RX2p	
31	GND	

----- Module Card Edge -----

Bottom Side (viewed from bottom)

	GND	1
	TX2p	2
	TX2n	3
	GND	4
	TX4p	5
	TX4n	6
	GND	7
	TX6p	8
	TX6n	9
	GND	10
	TX8p	11
	TX8n	12
	GND	13
	SCL	14
	VCC	15
	VCC	16
	LPWn/PRSn	17
	GND	18
	RX7n	19
	RX7p	20
	GND	21
	RX5n	22
	RX5p	23
	GND	24
	RX3n	25
	RX3p	26
	GND	27
	RX1n	28
	RX1p	29
	GND	30

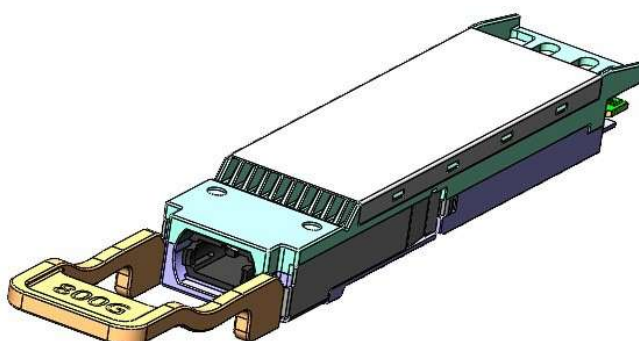
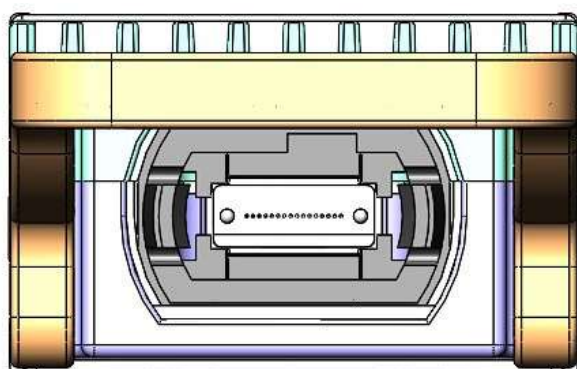
► Module contact definition

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVC MOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

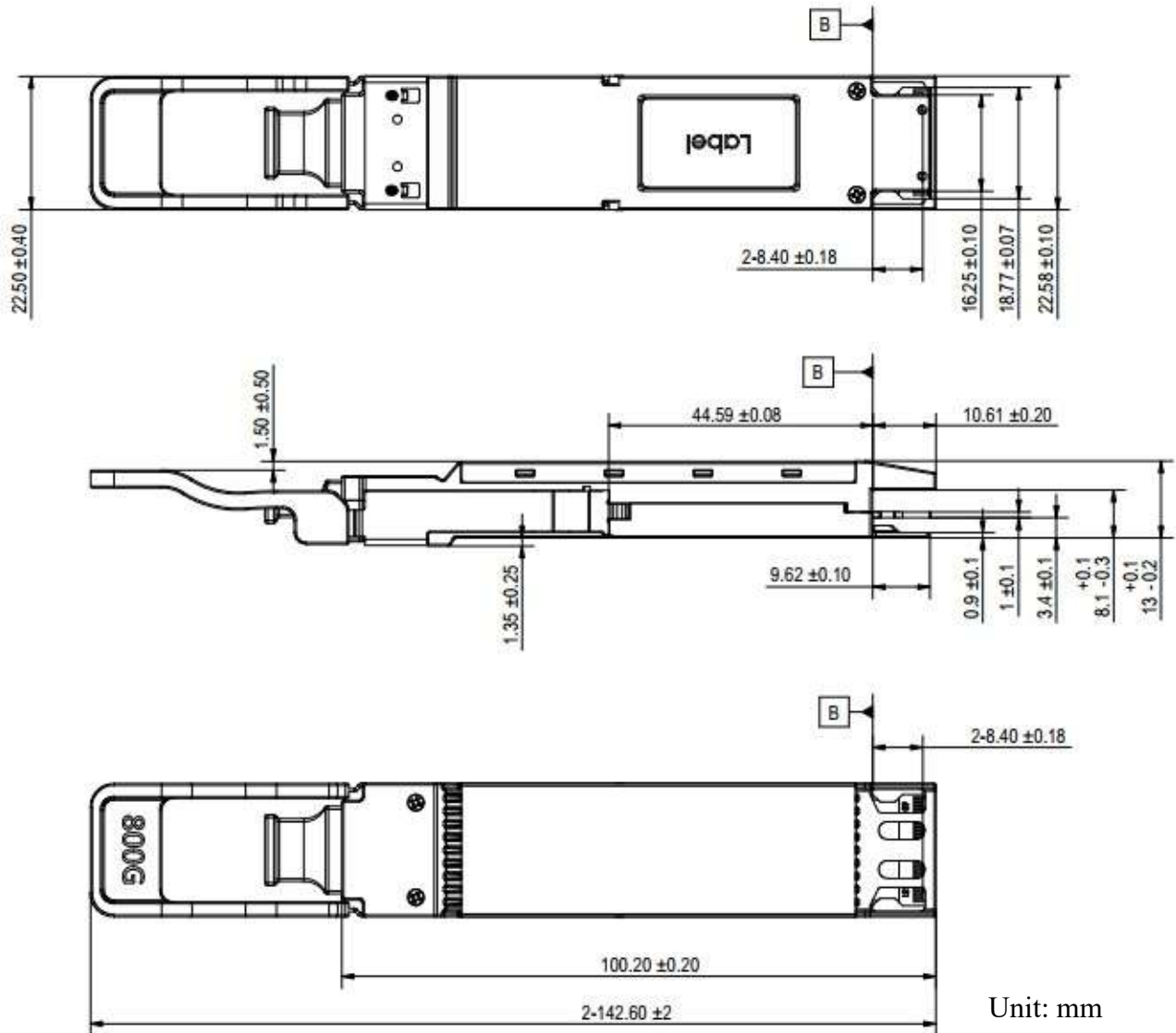
Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVC MOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

► Optical interface

The MPO16-APC connectors for OSFP800 SR8 LPO.



► Mechanical Specifications



Unit: mm

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