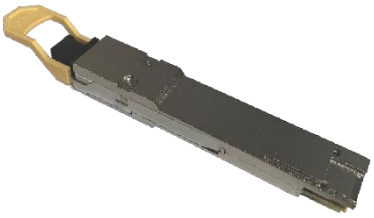
Hot Pluggable, Duplex LC,
+3.3V 850nm VCSEL-LD

# 800G LPO SR8 Optical Transceiver (STC-40028) Datasheet



- Hot-pluggable QDD800 800G form factor
- Single +3.3V power supply

## Applications:

- Data centers and Cloud Networks

## Features:

- Up to 106 Gbps data rate per channel by PAM4 modulation
- Support 800GAUI-8 electrical interface
- Integrated 850nm VCSEL array and PD array
- w/o DSP or CDR
- Up to 20m transmission with OM3 MMF
- Up to 50m transmission with OM4 MMF
- DDM function implemented

## Standards

- Compliant to QSFP-DD800 HW Rev 6.2
- Compliant to IEEE P802.3db
- Compliant with CMIS 4.0
- 8x106. 25Gb/s electrical interface (800GAUI-8)
- Maximum power consumption 5.5W
- Single +3.3V power supply
- Case temperature range: 0 ~ +70℃
- RoHS 2.0 complaint

| Rev | Date | Modified by | Description |
|---|---|---|---|
| A | Jul 25,2023 | Vic | Initial Release |
| B | Jul 24,2024 | Vic | Update power dissipation and described |
| C | Aug 29,2024 | Vic | Add Electrical、optical characteristics |

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## ► Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Storage Temperature Range | $T_{STG}$ | -40 | +85 | ºC |
| Supply Voltage | $V_{CC}$ | 0.5 | 3.6 | V |
| Relative Humidity | RH | 5% to 95% non-condensing | | |

## ► Operating Conditions

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Case Temperature- Operating | $T_{CASE}$ | 0 | 70 | ℃ |
| Supply Voltage | $V_{CC}$ | 3.135 | 3.465 | V |
| Power Consumption | $P_{DISS}$ | | 5.5 | W |
| Pre-FEC Bit Error Ratio | | | $2.4x10^{-4}$ | |
| Link Distance over OM3 | | 0.5 | 20 | m |
| Link Distance over OM4 | | 0.5 | 50 | m |

## ► Optical Specifications

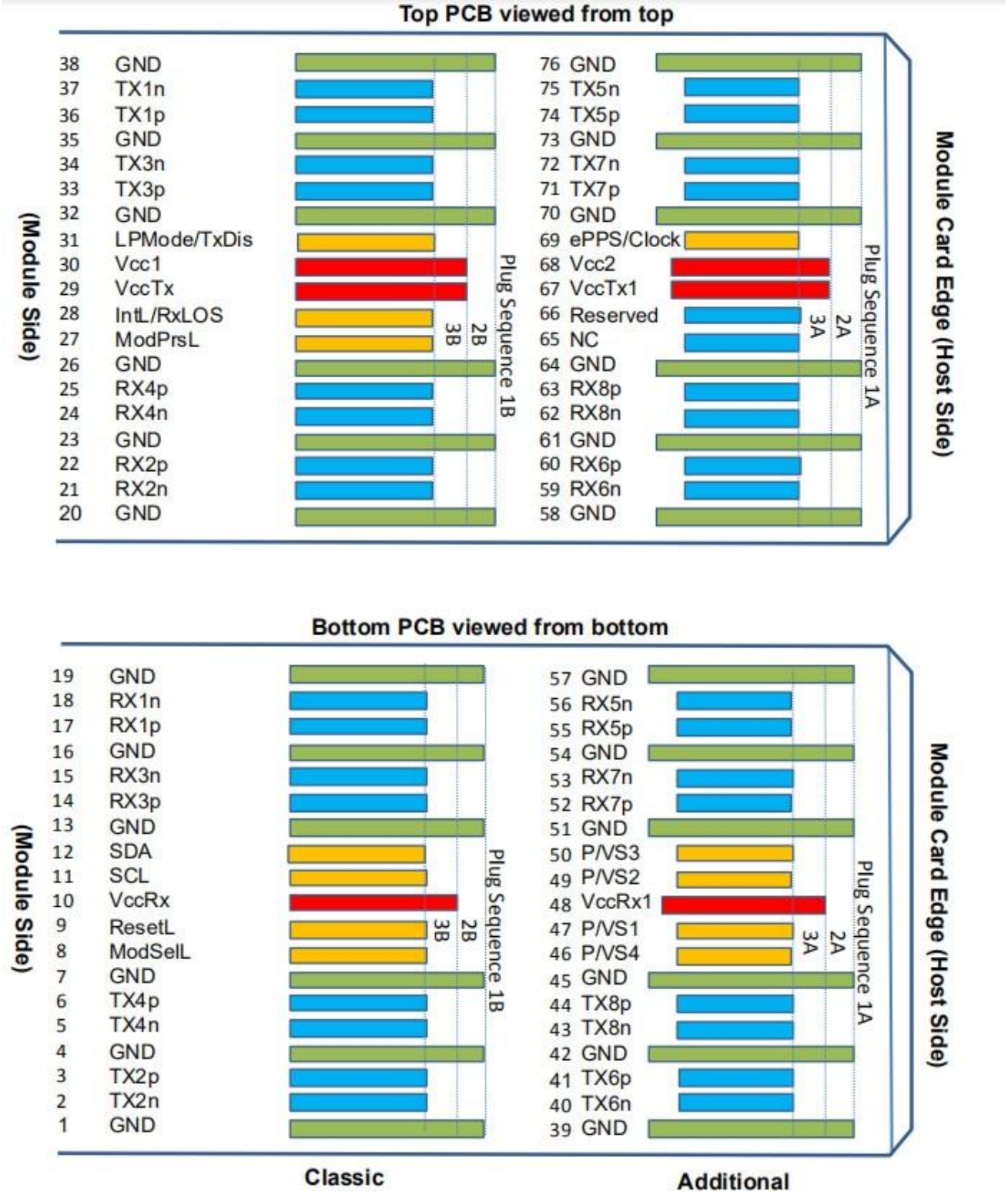
| Parameters | Units | Min | Max | Parameters |
|---|---|---|---|---|
| Tx/Rx signaling rate(each lane) | GBd | | 53.125 | |
| Tx_AOP | dBm | -4.6 | 4 | PRBS31Q |
| Tx_OMA (outer) | dBm | -2.6 | 3.5 | PRBS13Q |
| ER (outer) | dB | 2.5 | | PRBS13Q |
| TDECQ | dB | Golden sample approved | | SSPRQ pattern |
| OMA-TDECQ | dBm | | | |
| Tx/Rx wavelength range | nm | 840 | 870 | PRBS31Q |
| TxDisablePower | dBm | | -30 | |
| RIN17.1OMA | dB/Hz | | -132 | Square Wave |
| Optical return loss tol. | dB | | 17.1 | |
| Rx damage thresholde | dBm | 5 | | |
| Stressed_Sen_OMA@2E10 | dBm | Golden sample approved | | PRBS31Q |
| -4 | dBm | -6.4 | 4 | PRBS31Q |
| Rx_AOP | dBm | | 3.5 | PRBS13Q |
| Rx_OMA | dBm | Golden sample approved | | - |
| Sensitivity | dBm | -15 | -11 | |
| LOSA (OMA) | dBm | -14 | -10 | |
| LOSD (OMA) | dBm | 0.5 | 3 | |
| LOSH (OMA) | V | 3.036 | 3.565 | |
| DMI_VCC | dBm | -3 | 3 | |
| DMI_TX_Pwr_Err | dBm | -3 | 3 | |
| DMI_RX_Pwr_Err | °C | -3 | 3 | |
| DMI_Temp_Err | V | -0.1 | 0.1 | |

## ► 4. Electric Ports Definition

| Parameter | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|
| **Module-to-host electrical specifications (module output)** | | | | |
| Signaling rate, each lane (each lane) | | 53.125 | GBd | |
| Differential output voltage, pk-pk<br>Short mode<br>Long mode | | <br>500<br>845 | <br>mV mV | Host may request short or long modes, see IEEE Std. Annex 120G.5.1 |
| VMA<br>Short mode Long mode | <br>200<br>350 | | <br>mV mV | See OIF CEI 3.9, for both short and long modes |
| Common Mode Voltage (Vcm) | -350 | 2850 | mV | See note 2 |
| Peak to Peak AC Common Mode Voltage Low-frequency (VCMLF) | - | 32 | mV | See note 1 |
| Peak to Peak AC Common Mode Voltage Full-band (VCMFB) | - | 80 | mV | See note 1 |
| Differential Termination Resistance Mismatch | - | 10 | % | At 1 MHz, See OIF CEI 13.3.6 |
| Common Mode to Differential Mode Conversion (SDC22) | - | See OIF CEI Equation 2 | dB | See note 3 |
| Effective Return Loss (ERL) | 9 | - | dB | See note 4 |
| Common Mode Return Loss (SCC22) | | -2 | dB | From 250 MHz to min(0.8*fb, 42 GHz), See Note 3 |
| EECQ (Short and Long Modes) | | 10 | dB | See OIF CEI 4.1 and 4.2, See also Note 5 |

**NOTES:**
See IEEE Std 802.3 Table 120G-1 [4].
Vcm is generated by the host. Specification includes effects of ground offset voltage.
S-parameter specifications are based on a differential reference impedance of 100 Ω and a common mode reference impedance of 25 Ω.
See OIF CEI 3.12.
Reference equalizer for Short and Long Modes near-end eye measurement is 22 tap FFE and 1 tap DFE.
Reference equalizer for Short and Long Modes far-end eye measurement is Continuous Time Linear Equalizer (CTLE), 22 tap FFE and 1 tap DFE, See OIF CEI 4.5

## ► Pin Description



## ► Module contact definition

**Pad Function Definition**

| Pad | Logic | Symbol | Description | Plug Sequence[4] | Notes |
|---|---|---|---|---|---|
| 1 | | GND | Ground | 1B | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3B | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3B | |
| 4 | | GND | Ground | 1B | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3B | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3B | |
| 7 | | GND | Ground | 1B | 1 |
| 8 | LVTTL-I | ModSelL | Module Select | 3B | |
| 9 | LVTTL-I | ResetL | Module Reset | 3B | |
| 10 | | VccRx | +3.3V Power Supply Receiver | 2B | 2 |
| 11 | LVCMOS-I/O | SCL | TWI serial interface clock | 3B | |
| 12 | LVCMOS-I/O | SDA | TWI serial interface data | 3B | |
| 13 | | GND | Ground | 1B | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3B | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3B | |
| 16 | | GND | Ground | 1B | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3B | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3B | |
| 19 | | GND | Ground | 1B | 1 |
| 20 | | GND | Ground | 1B | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3B | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3B | |
| 23 | | GND | Ground | 1B | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3B | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3B | |
| 26 | | GND | Ground | 1B | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | 3B | |
| 28 | LVTTL-O | IntL/ RxLOS | Interrupt/optional RxLOS | 3B | |
| 29 | | VccTx | +3.3V Power supply transmitter | 2B | 2 |
| 30 | | Vcc1 | +3.3V Power supply | 2B | 2 |
| 31 | LVTTL-I | LPMode/ TxDis | Low Power mode/optional TX Disable | 3B | |
| 32 | | GND | Ground | 1B | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3B | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3B | |
| 35 | | GND | Ground | 1B | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3B | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3B | |
| 38 | | GND | Ground | 1B | 1 |
| 39 | | GND | Ground | 1A | 1 |
| 40 | CML-I | Tx6n | Transmitter Inverted Data Input | 3A | |
| 41 | CML-I | Tx6p | Transmitter Non-Inverted Data Input | 3A | |
| 42 | | GND | Ground | 1A | 1 |
| 43 | CML-I | Tx8n | Transmitter Inverted Data Input | 3A | |
| 44 | CML-I | Tx8p | Transmitter Non-Inverted Data Input | 3A | |
| 45 | | GND | Ground | 1A | 1 |

**Figure 1 MSA-compliant connector**

| Pad | Logic | Symbol | Description | Plug Sequence[4] | Notes |
|---|---|---|---|---|---|
| 46 | LVCMOS /CML-I | P/VS4 | Programmable/Module Vendor Specific 4 | 3A | 5 |
| 47 | LVCMOS /CML-I | P/VS1 | Programmable/Module Vendor Specific 1 | 3A | 5 |
| 48 | | VccRx1 | 3.3V Power Supply | 2A | 2 |
| 49 | LVCMOS /CML-O | P/VS2 | Programmable/Module Vendor Specific 2 | 3A | 5 |
| 50 | LVCMOS /CML-O | P/VS3 | Programmable/Module Vendor Specific 3 | 3A | 5 |
| 51 | | GND | Ground | 1A | 1 |
| 52 | CML-O | Rx7p | Receiver Non-Inverted Data Output | 3A | |
| 53 | CML-O | Rx7n | Receiver Inverted Data Output | 3A | |
| 54 | | GND | Ground | 1A | 1 |
| 55 | CML-O | Rx5p | Receiver Non-Inverted Data Output | 3A | |
| 56 | CML-O | Rx5n | Receiver Inverted Data Output | 3A | |
| 57 | | GND | Ground | 1A | 1 |
| 58 | | GND | Ground | 1A | 1 |
| 59 | CML-O | Rx6n | Receiver Inverted Data Output | 3A | |
| 60 | CML-O | Rx6p | Receiver Non-Inverted Data Output | 3A | |
| 61 | | GND | Ground | 1A | 1 |
| 62 | CML-O | Rx8n | Receiver Inverted Data Output | 3A | |
| 63 | CML-O | Rx8p | Receiver Non-Inverted Data Output | 3A | |
| 64 | | GND | Ground | 1A | 1 |
| 65 | | NC | No Connect | 3A | 3 |
| 66 | | Reserved | For future use | 3A | 3 |
| 67 | | VccTx1 | 3.3V Power Supply | 2A | 2 |
| 68 | | Vcc2 | 3.3V Power Supply | 2A | 2 |
| 69 | LVCMOS-I | ePPS/Clock | 1PPS PTP clock or reference clock input | 3A | 6 |
| 70 | | GND | Ground | 1A | 1 |
| 71 | CML-I | Tx7p | Transmitter Non-Inverted Data Input | 3A | |
| 72 | CML-I | Tx7n | Transmitter Inverted Data Input | 3A | |
| 73 | | GND | Ground | 1A | 1 |
| 74 | CML-I | Tx5p | Transmitter Non-Inverted Data Input | 3A | |
| 75 | CML-I | Tx5n | Transmitter Inverted Data Input | 3A | |
| 76 | | GND | Ground | 1A | 1 |

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500 mA.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500 mA.

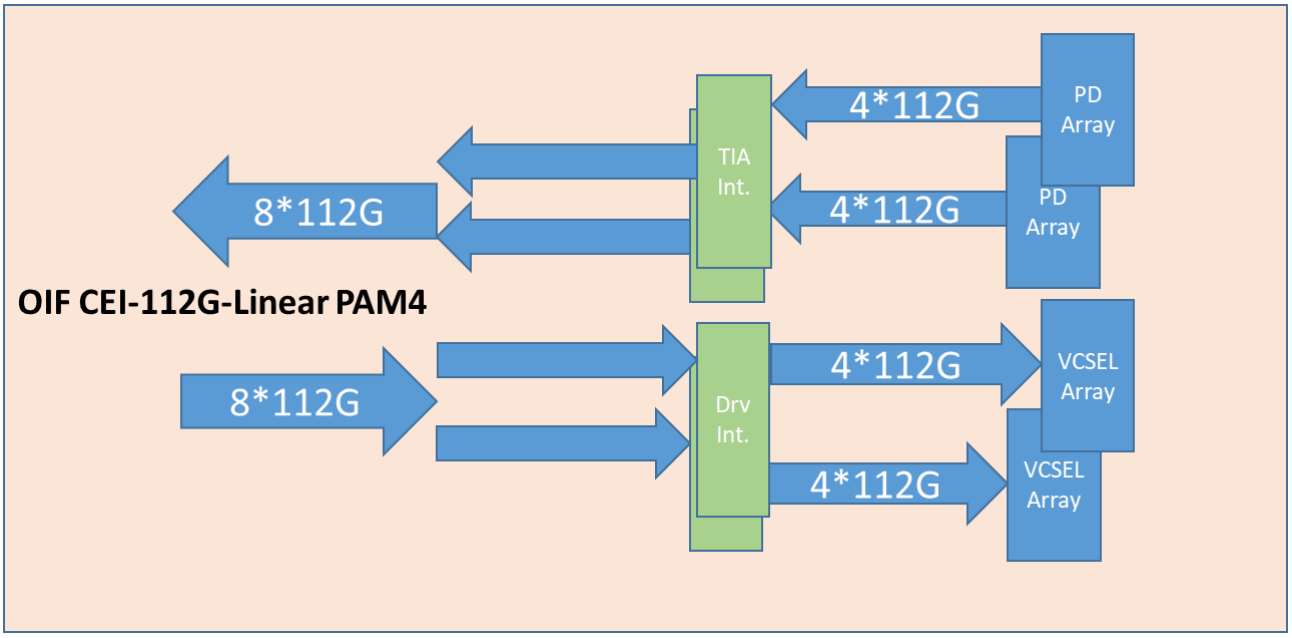
Note 3: Reserved and no Connect pads recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note 5: Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10 kΩ.

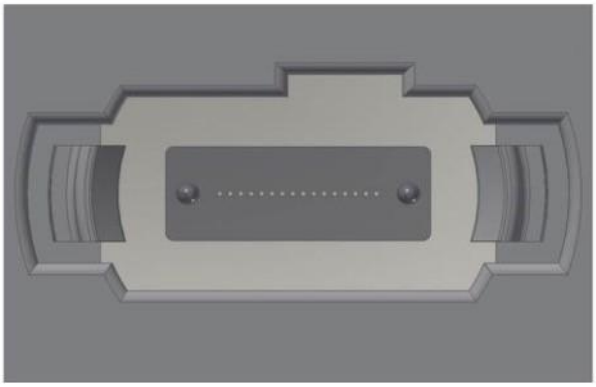
Note 6: ePPS/Clock if not used recommended to be terminated with 50 Ω to ground on the host.

## ► Module Block Diagram




## ► Optical interface

The eight transmit and eight receive optical lanes of the module occupy the positions depicted in Figure 3 when looking into the MPO16 receptacle with the connector keyway feature on top. The transmit optical lanes occupy the left-most eight positions. The receive optical lanes occupy the right-most eight positions.



## ► Mechanical Specifications